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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,553	09/15/2003	Yoichi Sato	03500.017560	9044

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FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
MCCOMMAS, BRENDAN N	
ART UNIT	**PAPER NUMBER**
2609	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,553	SATO, YOICHI	
	Examiner	Art Unit	
	Brendan N. McCommas	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 09/15/2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/661553.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (United States Patent 7,221,400) hereinafter referenced as Takahashi in view of Orava et al. (United States Patent 5,812,191) hereinafter referenced as Orava.

3. Regarding claim 1, Takahashi discloses a sensor device for automatic exposure and automatic focus. In addition, Takahashi discloses, in column 4, lines 43-51, that the analog and digital circuit blocks 105 and 106 in figure 2 control the power to the AE sensor photo diodes, which reads on the claimed power supply unit. In addition Takahashi discloses in columns 6, lines 39-64 and 10, lines 19-30, that the power supply circuits 105 and 106 control the AF (Auto-Focus) sensor circuits, which read on the claimed pixel area, independently of the AE (Auto-Exposure) sensor circuits based on signals sent to the digital circuit block 106.

4. Further, Takahashi discloses a control circuit, in column 7, lines 15-37, which independently controls the power supply to the Auto-Exposure circuits and the Auto-Focus circuits at a specified time, on the same semi-conductor substrate, which reads on claimed control circuit which supplies power to the different portions in a predetermined period after starting photo charge accumulation.

5. However Takahashi fails to disclose that the image pickup apparatus has a common output portion, controlled by the power supply unit.

6. However the examiner maintains that it was well known in the art for an imaging pickup apparatus to have a common output portion, controlled by a power supply unit as taught by Orava.

7. Orava discloses a semiconductor imaging device. Regarding the common output portion, Orava discloses, in column 2 lines 27-35, that the semiconductor imaging device has an array of pixel cells including a semiconductor detector substrate and a semiconductor read out substrate, which are both integral to the semiconductor substrate, wherein:

8. The semiconductor readout substrate includes an array of individually addressable pixel circuits, each of which is connected to a corresponding pixel detector cell to form a pixel cell, which reads on claimed, "common output portion for sequentially amplifying and outputting signals from the plurality of pixels included in said pixel area."

9. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the power control unit as disclosed in Takahashi by specifically providing a common output portion, and independently controlling the semiconductor read-out substrate with the power supply control unit in order to reduce current consumption as taught by Orava.

10. Regarding claim 2, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 1), in addition, Takahashi discloses in column 6, lines 39-51, the power supply control circuitry as shown in figures 1A and 1B, wherein

the said power control circuitry variably controls the timing of the AF sensors, either being in the operating or non-operating state, as disclosed in column 10, lines 19-30, which reads on claimed "control circuitry which variably controls the period during which no power is supplied to said common output portion."

11. Regarding claim 3, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 1), in addition, Takahashi discloses in figures 1A and 1B that the power control circuitry (105a, 105b, and 105c) is on the semiconductor substrate (100) which reads on claimed, "power supply unit is formed on said single semiconductor substrate."

12. Regarding claim 4, Takahashi discloses a sensor device for automatic exposure and automatic focus. In addition, Takahashi discloses, in column 4, lines 43-51, that the analog and digital circuit blocks 105 and 106 in figure 2 control the power to the AE sensor photo diodes, by using a control signal at either an intermediate level, or a VDD level, as disclosed in column 10, lines 19-30, which reads on the claimed power supply unit outputting first and second voltage levels.

13. Further, Takahashi discloses a control circuit, in column 7, lines 15-37, which independently supplies power at different levels to the Auto-Exposure circuits and the Auto-Focus circuits at a specified time on the same semi-conductor substrate, which reads on claimed control circuit which supplies power to the different portions in a predetermined period after starting photo charge accumulation.

14. However Takahashi fails to disclose that the power supply unit supplies two different voltage levels to the common output portion,

15. However the examiner maintains that it was well known in the art for an imaging pickup apparatus to have a power supply unit, supplying different power levels to the common output portion, as taught by Orava.

16. Orava discloses a semiconductor imaging device. Regarding the common output portion, Orava discloses, in column 2 lines 27-35, that the semiconductor imaging device has an array of pixel cells including a semiconductor detector substrate and a semiconductor read out substrate, which are both integral to the semiconductor substrate, wherein:

17. The semiconductor readout substrate includes an array of individually addressable pixel circuits, each of which is connected to a corresponding pixel detector cell to form a pixel cell, which reads on claimed, "common output portion for sequentially amplifying and outputting signals from the plurality of pixels included in said pixel area."

18. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the power control unit as disclosed in Takahashi by specifically providing a common output portion, and independently controlling the semiconductor read-out substrate with the power supply control unit in order to reduce current consumption as taught by Orava.

19. Regarding claim 5, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 4), in addition, Takahashi discloses in column 6, lines 39-51, the power supply control circuitry as shown in figures 1A and 1B, wherein the said power control circuitry variably controls the timing of the AGC, by using a control signal at either an intermediate level, or a VDD level, as disclosed in column 10,

lines 19-30, which reads on claimed "control circuitry which variably controls the period during which the second power level is supplied to said common output portion."

20. Regarding claim 6, Orava and Takahashi, the combination discloses everything claimed as applied above (see claim 4), in addition, Takahashi discloses in figures 1A and 1B that the power control circuitry (105a, 105b, and 105c) is on the semiconductor substrate (100), which reads on, claimed, "power supply unit is formed on said single semiconductor substrate."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brendan N. McCommas whose telephone number is 571-270-3575. The examiner can normally be reached on M-F (alternate F off) 7:30 am -5 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jefferey Harold can be reached on 571-272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brendan N McCommas
Examiner
Art Unit 2609

BM
BM
August 16, 2007

JEFFEREY F. HAROLD
SUPERVISORY PATENT EXAMINER